IJREAT International Journal of Research in Engineering & Advanced Technology, Volume 1, Issue 1, March, 2013
ISSN: 2320 - 8791
www.ijreat.org

Asymmetric Thirteen Level Grid connected Inverter for Photovoltaic System

N.SRINIVASAN
Department of Electrical and Electronics Engineering
Vel Tech Dr.Rr & Dr.Sr Technical University Avadi Chennai-600062

Abstract

This paper proposes a single- phase thirteen -level inverter for grid-connected photovoltaic system with novel pulse width modulated (PWM) control scheme. A reference with an offset that is equivalent to the amplitude of the carrier signal was used to generate the PWM signals. The inverter is capable of producing thirteen levels of output-voltage levels from the dc supply voltage. The proposed system was verified through simulation and Hardware.

Index Terms—Grid connected, modulation index, multilevel inverter, photovoltaic (PV) system, pulse modulated (PWM), Total harmonic distortion (THD).

1.Introduction

The ever-increasing energy consumption, fossil fuels soaring costs and exhaustible nature, and worsening global environment have created a booming interest in renew-able energy generation systems, one of which is photovoltaic. Such a system generates electricity by converting the Sun's energy directly into electricity. Photovoltaic-generated energy can be delivered to power system net works through grid-connected inverters.

A single phase grid connected inverter usually used for residential or low power applications of power ranges that are less than 10 Kw. Types of single phase grid connected inverter can satisfy specifications through its very high switching, but it could also unfortunately increases switching losses, acoustic noise, and level of interference equipment. Improving output waveform reduce its harmonic content and, and hence, also size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation.

Multilevel inverters are promising, they have nearly sinusoidal output voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact. Various topologies for multilevel inverter have been proposed over the years. Common one is diode clamped, flying capacitor, cascaded H-bridge and modified H-bridge multilevel. This paper recounts the development of a thirteen level inverter that has three diodes, seven switches and PWM technique.

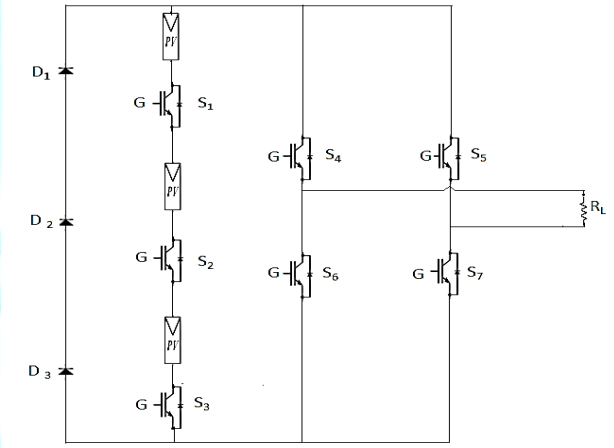


Fig.1. Proposed multi level inverter topology

2.System Design

T he proposed system is capable of producing thirteen level of output which can be connected to the grid. It comprises a single phase inverter, three diodes, and seven switches shown in Fig.1.

The modified inverter topology is significantly advantageous over other topologies i.e. less power switches, power diodes, and no capacitors used for the same inverters of the same number of levels.

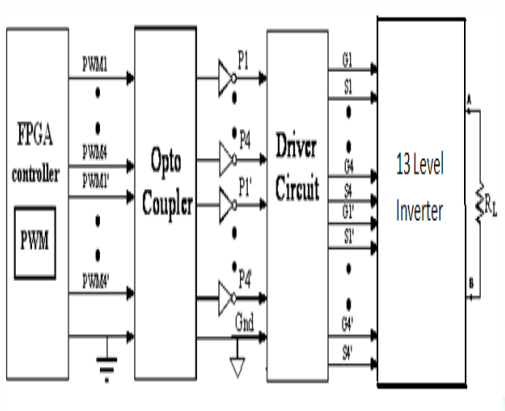


Fig.2. Proposed Block diagram of inverter topology

The basic block diagram of the inverter system consist of user interface, switching pattern generation unit, driver circuit, power supply, power circuit, and the output unit.

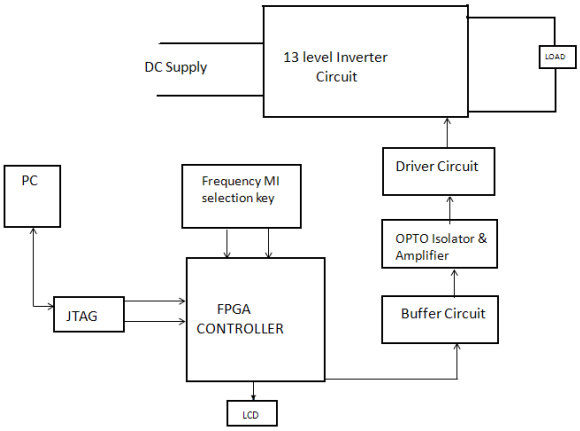


Fig.3. Functional block diagram of FPGA

An FPGA is a regular structure of logic cells or modules and interconnect which is under the designer's complete control. This means the user can design, program and make changes to his circuit whenever he wants.
Field Programmable Gate Arrays (FPGAs), as the name suggests these devices are a uniform array of gates that can be updated by the designer on the board as and when required. In some cases these devices are known as ASICs (Application Specific Integrated Circuits), that is each device is configured by the designer to perform a function particular to his application. In most ASIC technologies, gate level interconnections are established when the device is manufactured (i.e. custom and semi-custom ASICs).
FPGA Advantage
1. Enhanced flexibility
2. Reduced board space, power and cost
3. Increased performance

All FPGAs have the following key elements:
The Programming technology, basic logic cells, I/O logic cells, Programmable interconnect, Software to design and program the FPGA

3. SPARTAN-3 EFPGA

The Spartan™-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates, as shown in Table. The Spartan-3E family builds on the success of the earlier Spartan-3 family by increasing the amount of logic per I/O, significantly reducing the cost per logic cell. New features improve system performance and reduce the cost of configuration. These Spartan-3E enhancements, combined with advanced 90 nm process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry. Because of their exceptionally low cost, Spartan-3E FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment. The Spartan-3E family is a superior alternative to mask programmed Asics. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, impossibility with ASICs.

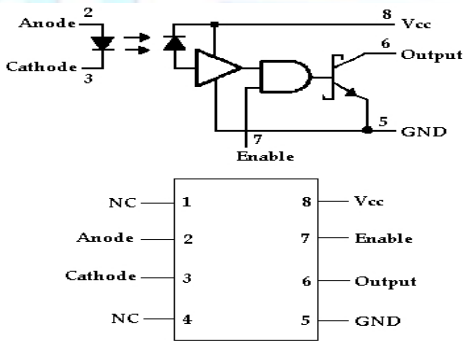


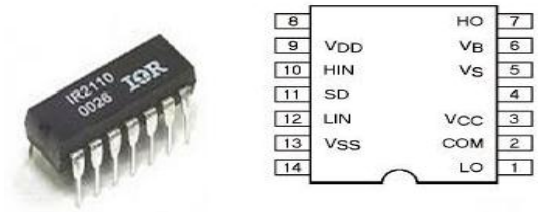
Fig.4. SPARTAN-3 EFPGA

3.1 Opto coupler

The function of an Opto isolator is to isolate the control circuit from the power Circuit. The name of this opto coupler IC is 6N137.

3.2 Gate driver

Gate driver acts as high power buffer stage between the PWM control device and gates of the primary power switching Devices likes as MOSFET, IGBT.



Fi. 5. PIN Diagram

4.Pulse width Modulation

A PWM waveform is a sequence of pulses with fixed frequency but varying pulse widths. The width of the pulse might vary from 0% to 100% of the fixed period.

Types of PWM: Single PWM, Multiple PWM, Sine PWM, Space Vector PWM.

The diagram shows how comparing a ramping waveform with a DC level produces the PWM waveform that we require. The DC signal can range between the minimum and maximum voltages wave of the triangle.

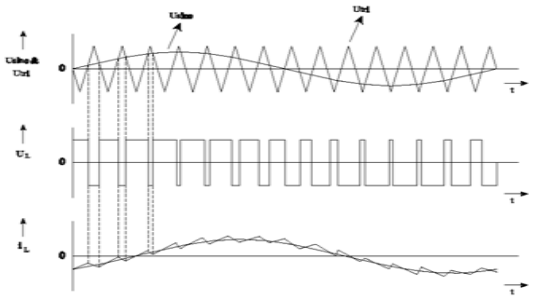


Fig. 6.Pulse Width Modulation

When the triangle waveform voltage is greater than the DC level, the output of the op-amp swings high, and when it is lower, the output swings low. The sinusoidal waveform is compare to the Carrier (Triangular wave) signal; the Comparator output PWM is called SPWM.

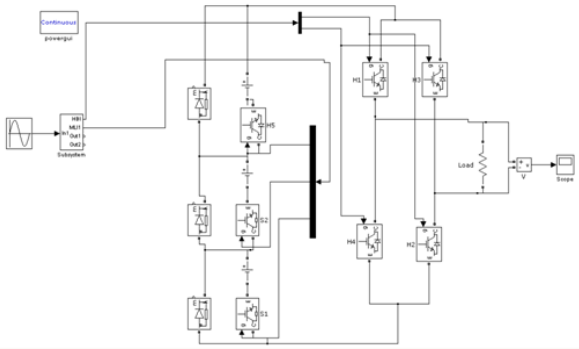


Fig. 7.Simulation Diagram for Proposed System

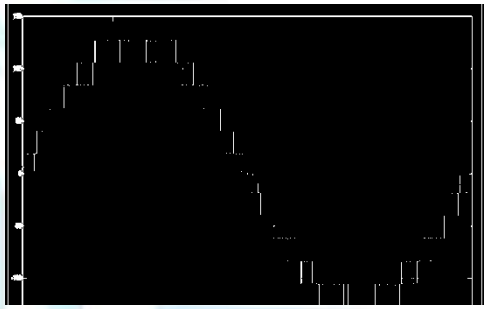
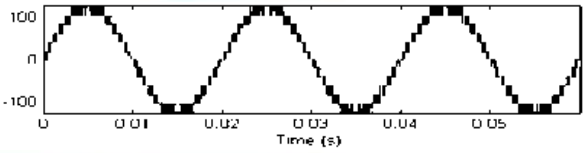
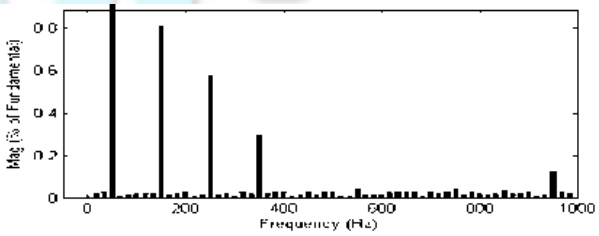


Fig.**8** Simulation Results

FFT AND THD VALUES



Fundamental frequency(50 Hz),THD=9.27%



4.1 Applications

- Emergency lighting systems
- Variable speed drives
- Uninterrupted power supplies
- Frequency converter

5.Conclusion

Therefore the single phase thirteen level inverter switching losses reduced by having less number of power switches and THD value obtained is 9.27%.

6.References

[1] A. Nabae, I. Takahashi, H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," IEEE Trans. Industry Applications, vol. IA-17, no. 5, Sept.1981, pp. 518-523.

[2] J. K. Steinke, "Control Strategy for a Three Phase AC Traction Drive witha 3-Level GTO PWM Inverter," IEEEPESC, 1988, pp. 431-438.

[3]G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, G. Sciutto, "A NewMultilevel PWM Method: A Theoretical Analysis,"
IEEE Trans. PowerElectronics, vol. 7, no. 3, July 1992, pp. 497-505.

[4] R. W. Menzies, P. Steimer, J. K. Steinke, "Five-Level GTO Inverters for Large Induction Motor Drives," IEEE Trans. Industry Applications,
vol.30, no. 4, July 1994, pp. 938-944.

[5] R. W. Menzies, Y. Zhuang, "Advanced Static Compensation Using a
Multilevel GTO Thyristor Inverter," IEEE Trans. Power Delivery, April
1995, pp. 732-738.

[6]Y. Chen, B. Mwinyiwiwa, Z. Wolanski, B. T. Ooi, "Regulating and
Equalizing DC Capacitance Voltages in Multilevel STATCOM,"
IEEETrans. Power Delivery, vol. 12, no. 2, April 1997, pp. 901-907.

[7]N. S. Choi, J. G. Cho, G. H. Cho, "A General Circuit Topology of
Multilevel Inverter," IEEE PESC,1991, pp. 96-103.
IEEE IAS 1998 Annual Meeting, St. Louis, Missouri, October 10-15, 1998, pp. 1424-1431.

[8]N. S. Choi, G. C. Cho, G. H. Cho, "Modeling and Analysis of a Static VarCompensator Using Multilevel Voltage Source Inverter,"
IEEE IASAnnual Meeting, 1993, pp. 901-908.

[9]V. G. Agelidis, M. Calais, "Application Specific Harmonic Perfor-manceEvaluation of Multicarrier PWM Techniques,"IEEE PESC, 1998, pp.172-178.

[10]
M. Fracchia, T. Ghiara, M. Marchesoni, M. Mazzucchelli, "Optimized
Modulation Techniques for the Generalized N-Level Converter,"
IEEEPESC, 1992, pp. 1205-1213.

[11]H. L. Liu, G. H. Cho, "Three-Level Space Vector PWM in Low Index
Modulation Region Avoiding Narrow Pulse Problem,"
IEEE Trans. PowerElectronics,vol. 9, no. 5, Sept. 1994, pp. 481-486.

[12]G. Sinha, T. A. Lipo, "A Four Level Rectifier-Inverter System for DriveApplications," IEEE IAS Annual Meeting, 1996, pp. 980-987

[13]M. H. Ohsato, G. Kimura, M. Shioya, "Five-Stepped PWM Inverter Usedin Photovoltaic Systems," IEEE Trans. Industrial Electronics
, vol. 38, no.5, Oct. 1991, pp. 393-397.

[14]G. Carrara, D. Casini, S. Gardella, R. Salutari, "Optimal PWM for the
Control of Multilevel Voltage Source Inverter,"Fifth Annual European
Conference on Power Electronics, vol. 4, 1993, pp. 255-259.

[15]D. G. Holmes, "The Significance of Zero Space Vector Placement for
Carrier Based PWM Schemes,"IEEE IAS Annual Meeting, 1995, pp.
2451-2458.

[16]L. M. Tolbert, F. Z. Peng, "Multilevel Converters for Large Electric
Drives," IEEE APEC, 1998, pp. 530-536.